XUANTIE

Datasheet

XuanTie E901+

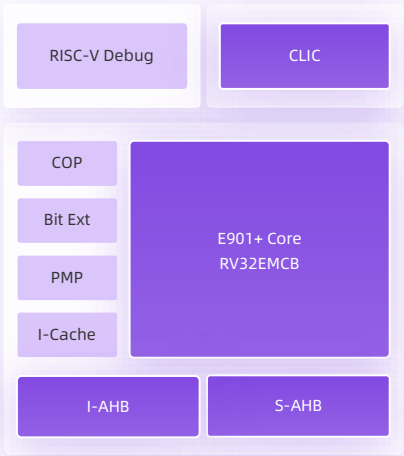
Most Area Efficiency Processor

Overview

The XuanTie E901+ processor is a fully synthesizable, highly area-efficient and energy-efficient RISC-V processor for embedded market.

The XuanTie E901+ processor supports the RV32E[M]C[B] instruction set architecture, featuring a mixed 16-bit/32-bit encoding system. The E901+ processor has a two-stage pipeline and custom coprocessor interface, which accelerates the execution of specific applications by supporting custom instructions.

The E901+ processor is designed for embedded applications such as smart cards, mini MCU, and IoT connectivity.



Features

Feature	Description
Architecture	RV32EMCB
Execution mode	Machine mode and user mode
Bus interface	AMBA3 AHB or AHB-Lite 32-bit master, and 2nd AHB interface
Pipeline	2-stage
PMP region	0, 2, 4, 8, or 16 regions
Instruction cache	Up to 8KB (optional)
Coprocessor	Coprocessor interface (optional)
Interrupt	Up to 112 interrupts, support NMI
Sleep mode	Sleep mode and deep sleep mode
Debug	2-wire or 5-wire JTAG debug port Hardware and software breakpoints

XuanTie E901+ Components

Processor Overview

The XuanTie E901+ processor adopts a 16/32 bits mixed instruction set and implements an energy-efficient 2-stage, single issue and in-order execution integer pipeline. Besides, the E901+ processor customizes two cache instructions and a few extended CSRs to support the extensions.

Core Local Interrupt Controller (CLIC)

The E901+ processor implements the RISC-V standard interrupt controller, CLINT and CLIC. The CLIC function has the following features:

- Up to 112 external interrupts
- Up to 32 priority settings
- Support level or positive/negative edge interrupt types
- Support hardware vector interrupt
- Control registers are memory mapped

Instruction Cache

The E901+ processor implements an optional instruction cache, which can cache data from the instruction bus such as Flash or I-SRAM. The instruction cache has the following features:

- 2-way set-associative
- FIFO cache replacement policy
- Can be configured to 2KB, 4KB, or 8KB

Physical Memory Protection (PMP)

The E901+ processor optionally supports RISC-V PMP, which allows machine and user privilege modes to access different address ranges. Only the machine mode has the authority to define the memory access permissions. If an unauthorized access is detected, an access fault exception is triggered. The PMP function has the following features:

- Up to 16 regions can be configured
- Read/Write/Execution memory protection
- Minimum 4KB address range

Debug Components

The E901+ processor adopts 2-wire debug port or 5-wire JTAG to communicate between the host and E901+ debug unit. The debug unit supports the following operations:

- Support hardware/software breakpoint
- Support hardware watchpoint
- Check and modify CPU register resource

- Support single step and multi-step debugging flexibly
- Speed up program download though 2-wire debug port or standard 5-wire JTAG port

Interface

The E901+ processor has one 32-bit AMBA3 AHB or AHB-Lite master bus to communicate with the external memory or peripheral IP. It also supports a second 32-bit AMBA3 AHB interface.

Coprocessor

The E901+ processor has an optional coprocessor interface that engineers could leverage for custom instruction design.

Control Extension

The E901+ processor implements the following control features:

- Support NMI
- Support lockup
- Support sleep and deep sleep modes
- Support soft reset operation
- Support configurable reset address through top port during integration
- Extend two cache instructions besides the standard RV32 ISA

Processor Configuration Options

The XuanTie E901+ processor provides feature configuration options, which can be set during integration.

Feature	Options
Architecture	RV32E[M]C[B]
Hardware multiplier	When multiplier is chosen, MAD is either one cycle multiplier or shift-add multiplier
Hardware division	When multiplier is chosen, hardware division is supported
PMP region	0, 2, 4, 8, or 16
Instruction cache	Up to 8KB (optional)
Coprocessor	Present or not
B extension	Present or not
Interrupt	1~112
Hardware breakpoint number	1, 4, or 8
Debug port	2-wire or 5-wire debug port JTAG

Software Ecosystems

- Compiler, assembler, linker, debugger and binary tools are contributed to GNU/LLVM and supported officially
- QEMU is contributed and supported officially
- Code size optimized runtime library
- Integrated Development Environment (CDK)
- High speed of program downloader

Power, Performance and Area

Condition: TSMC 40LP 9TC50	
Performance	1.73 DMIPS/MHz 3.25 Coremark/MHz
Frequency	160MHz
Area	Start from 16.2K Gate
Power	Start from 2.24 uW/MHz