XUANTIE

Datasheet

XuanTie C908X

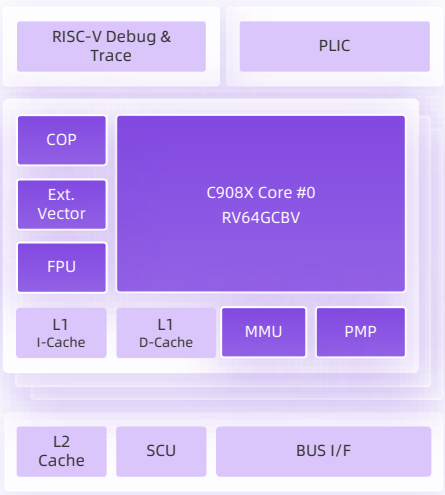
AI Enhanced Processor

Overview

The XuanTie C908X processor is a 64-bit RISC-V processor delivering high computational performance for running AI workloads.

Supporting up to 4096-bit bandwidth through the RVV extension and enhanced with dedicated AI instructions, the C908X processor accelerates AI computation efficiency.

The C908X processor is optimized for AI applications in terminals, edge devices, and infrastructure.



Features

Feature	Description
Architecture	RV64GCBV
ISA extension	XuanTie Instructions, AI Instructions
Execution mode	Machine, supervisor and user modes
Micro-arch	9-stage, in order, dual issue, branch prediction
Multi-core	Up to 4 cores per cluster
Bus interface	AMBA4 AXI master AMBA4 Low Latency Port (M-AXI4) AMBA4 Device Coherence Port (S-ACE) AMBA4 Fast memory interface (M-AXI4)
L1 Cache	16/32/64 KB Instruction cache with optional parity Data cache with optional ECC
L2 Cache	128/256/512/1024/1536/2048/3072/4096 KB With optional ECC

Features (cont.)

Feature	Description
Interrupt	PLIC + CLINT, up to 1023 interrupts
Data type	INT8/INT16/INT32/INT64, BF16/FP16/FP32
Vector	Extend from RVV, VLEN 512/1024/4096
PMP region	8, 16, 32, or 64 regions
SV/PA	SV39 or SV48 / PA40 or PA48
Coprocessor	Coprocessor interface (optional) to support XuanTie Custom Instructions
Sleep mode	Cluster or per core
Debug	RISC-V Debug
Trace	RISC-V Nexus Trace

XuanTie C908X Components

Processor Overview

The XuanTie C908X processor supports the RV64GCBV instruction set architecture. The C908X processor has nine-stage pipelines, an up to 4096-bit bandwidth RVV extension as well as additional AI instructions. The C908X processor supports up to 4 cores per cluster.

Core

- Nine-stage integer pipeline
- In-order, dual issue
- Branch prediction mechanisms

Multi-Core

- Support 1 ~ 4 SMP
- MOESI coherency protocol
- Generic interrupt controllers, timers and debug modules

Floating Point Unit

- RISC-V H, F, D extensions
- IEEE-754 compliant

Vector Extension

- RISC-V V Extension (RVV1.0)
- Support VLEN 512/1024/4096
- Support INT8/16/32/64, BF16/FP16/FP32
- Fast memory interface

Memory System

- L1 instruction cache: 4-way set-associative, optional parity, fixed 64-byte cache line length, optional 16/32/64KB
- L1 Data Cache: 4-way set-associative, optional ECC, fixed 64-byte cache line length, optional 16/32/64KB
- L2 Cache: 16-way set-associative, optional ECC, fixed 64-byte cache line length, optional 128/256/512/1MB/1.5MB/2MB/3MB/4MB

Physical Memory Protection (PMP)

Optional 8/16/32/64 regions

Memory Management Unit (MMU)

- SV39/SV48 virtual memory systems, support 40bit and 48bit physical addressing
- 16-entry fully associative uTLB

Platform level interrupt controller (PLIC)

- Support multi-core, multi-cluster interrupt control
- Support up to 1023 PLIC interrupt sources
- Support up to 32 PLIC interrupt priority levels
- Support 256 PLIC interrupt targets
- Edge trigger or level trigger

Debug Components

- RISC-V Debug
- Support multi-core debug
- Support hardware/software breakpoint
- Support hardware watchpoint
- Check and modify CPU register resource
- Single step or multi step flexibly supported
- Support program download though JTAG

Low Power Design

- WFI mechanism to put core into low power mode
- Support sub-module clock gating automatedly when idle
- Support per-core power down and cluster power down

Coprocessor

The XuanTie coprocessor interface introduces the XuanTie Custom Extension, a flexible, self-defined interface that allows customers to add custom instructions.

- Up to 3 source operands for custom scalar instruction
- Support either synchronization or asynchronization mechanism

Interface

The C908X processor implements interfaces listed below for control:

- AMBA4 M-AXI master
- AMBA4 Low Latency Port (M-AXI)
- AMBA4 Device Coherence Port (S-AXI)
- AMBA4 Fast memory interface
- Debug (JTAG)
- Interrupts

Processor Configuration Options

The XuanTie C908X processor provides feature configuration options, which can be set during integration.

Category	Feature	Options
Multi-core	Core number	1,2,3,4
Coprocessor	XuanTie Custom Instructions support	Present or not
MMU	MMU	Present or not
	Virtual memory address	39 or 48
PMP	EPMP	Present or not
	PMP_REGION	8,16,32,64
L1 I-Cache	Cache size (KB)	16,32,64
L1 D-Cache	Cache size (KB)	16,32,64
L1 cache ECC	L1 cache ECC	Present or not
RVV Extension	VLEN	512/1024/4096
	Fast memory interface	Present or not
	Vector AI extension	Present or not
Performance monitor	Performance monitor	Present or not
TEE	TEE extension	Present or not
Interrupt	Platform level Interrupt	Present or not
	Platform level Interrupt number	1~1023
L2 cache	L2 cache Size (KB)	128,256,512,1024, 1536,2048,3072,4096
	L2 cache ECC	Present or not
	L2 cache slice number	1 or 2
Snoop filter	L2 snoop filter size	16,32,64,128,256,512, 1024
	Double master	Present or not
Bus configuration	Main bus	AXI
	Bus width	128 or 256
	Low Latency Port	Present or not
Physical addressing	Physical addressing	40 or 48

Software Ecosystems

- OS kernel: Linux, freeRTOS, RT-Thread
- Compiler, assembler, linker, debugger and binary tools are contributed to GNU/LLVM and supported officially
- QEMU is contributed and supported officially
- Integrated Development Environment (CDK and CDS)
- Libraries: C908X-NNLib

Power, Performance and Area

	C908X 512b [1]	C908X 1024b [1]	C908X 4096b [2]
Frequency GHz, ssgnp0p72v125c	1.75	1.65	1.6
Power mW/GHz, Running SoftMax	183	383.6	1300
Area mm^2, per-core, not including PLIC/L2 memory system/trace and debug, before shrink	1.464	2.56	2.09

- Configuration: 4-core cluster, FPU, ECC, AI Extension, 32KB I-Cache/D-Cache, 128KB L2 Cache
- [1] Condition: TSMC 12FFC
- [2] Condition: SAMSUNG 4LPP